IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Confirmation No.: 3131
Lawrence M. BURNS	Art Unit: 2817
Patent. No.: 6,982,602 B2	Examiner: Henry Choe
Issued: January 3, 2006	Atty. Docket: 1875.1090008
For: **Low Voltage Input Current Mirror Circuit And Method**	

Request for Certificate of Correction Under 37 C.F.R. § 1.322

Attn: Certificate of Correction Branch

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

It is hereby requested that a Certificate of Correction under 37 C.F.R. § 1.322 be issued for the above-captioned United States Patent. This Certificate of Correction is being requested due to a mistake which appears in the printed patent. This mistake was made by the U.S. Patent and Trademark Office.

Specifically, the printed patent contains the following error for which a Certificate of Correction is respectfully requested:

In Claim 16, at column 15, line 20, "the current in response" should appear as

- - the input current in response - -.

A copy of Applicant's Amendment and Reply filed on September 1, 2004 is attached hereto in support of this correction, along with a copy of the date-stamped

postcard. Issued claim 16 corresponds to claim 30 as shown in the Amendment and Reply.

Remarks

The above-noted correction does not involve such changes in the patent as would constitute new matter or would require reexamination.

A completed Form PTO/SB/44 accompanies this request, with the above-noted correction printed thereon. Accordingly, a Certificate of Correction is believed proper and issuance thereof is respectfully requested.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

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		Due Date:	September 1, 2004
Applicants:	Lawrence M. BURNS.	**Art Unit:**	2817
		Examiner:	Henry CHOE
Application No.:	10/679,269	**Docket:**	1875.1090008
Filed:	October 7, 2003	**Atty:**	VLB
For:	**Low Voltage Input Current Mirror Circuit and Method**		

When receipt stamp is placed hereon, the USPTO acknowledges receipt of the following documents:

1. SKGF Cover Letter;
2. Fee Transmittal (PTO/SB/17);
3. Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(1);
4. Copy of executed Power of Attorney by Assignee;
5. Copy of executed Certificate Under 37 C.F.R. § 3.73(b) with a copy of the Assignment attached;
6. Terminal Disclaimer to Obviate a Double Patenting Rejection Over a Prior Patent (PTO Form PTO/SB/26);
7. Amendment and Reply Under 37 C.F.R. § 1.111;
8. Credit Card Payment Request (PTO-2038) in the amount of $1,060.00 for
   $950.00 Three (3) month extension of time; and
   $110.00 for Terminal Disclaimer Fee; and
9. One Return Postcard.

Mail Stop: Amendment

Please Date Stamp and Return to Our Courier

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3131
Lawrence M. BURNS	Art Unit: 2817
Appl. No.: 10/679,269	Examiner: Henry Choe
Filed: October 7, 2003	Atty. Docket: 1875.1090008
For: **Low Voltage Input Current Mirror Circuit And Method**	

Amendment and Reply Under 37 C.F.R. § 1.111

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the Office Action dated March 1, 2004, Applicant submits the following Amendment and Remarks. This Amendment is provided in the following format:

(A) Each section begins on a separate sheet;

(B) Starting on a separate sheet, amendments to the specification by presenting replacement paragraphs marked up to show changes made;

(C) Starting on a separate sheet, a complete listing of all of the claims:

- in ascending order;

- with status identifiers; and

- with markings in the currently amended claims;

(D) Starting on a separate sheet, the Remarks.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-14. (cancelled)

15. (new) An integrated circuit, comprising:

a substrate; and

a bias circuit, disposed on the substrate, for establishing a plurality of bias voltages from an input current supplied to an input terminal, the bias circuit comprising

an input stage adapted to establish a first bias voltage at the input terminal in response to the input current,

a current stage adapted to produce a bias current and a main mirror current each proportional to the input current in response to the first bias voltage and a second bias voltage,

a feedback stage adapted to produce a feedback current proportional to the input current in response to the bias current and the main mirror current, and

a reference bias stage adapted to establish the second bias voltage in response to the feedback current from the feedback stage, whereby the first and second bias voltages track the input current over variations in at least one of process, temperature and power supply voltage.

16. (new) The integrated circuit of claim 15, wherein the feedback stage of the bias circuit comprises:

a reference voltage stage adapted to establish third and fourth bias voltages in response to the bias current and the main mirror current; and

a current source adapted to produce the feedback current in response to the third and fourth bias voltages.

17. (new) The integrated circuit of claim 16, wherein the reference voltage stage of the bias circuit comprises:

a bias stage adapted to establish the third bias voltage in response to the bias current; and

a reference stage adapted to establish the fourth bias voltage in response to the main mirror current and the third bias voltage.

18. (new) The integrated circuit of claim 16, wherein the input stage and the reference bias stage are each constructed using transistors of a first type such that the first and second bias voltages are suitable for biasing current sources constructed using transistors of the first type, and wherein the reference voltage stage is constructed using transistors of a second type complementary to the first type such that the third and fourth bias voltages produced thereby are suitable for biasing current sources constructed using transistors of the second type.

19. (new) The integrated circuit of claim 16, wherein the reference voltage stage is constructed using p-type Metal Oxide Semiconductor (PMOS) transistors such that the third and fourth bias voltages established thereby are suitable for biasing one or more current sources constructed using PMOS transistors.

20. (new) The integrated circuit of claim 15, wherein the input stage and the reference bias stage are each constructed using n-type Metal Oxide Semiconductor (NMOS) transistors such that the first and second bias voltages established thereby are suitable for biasing one or more current sources constructed using NMOS transistors.

21. (new) The integrated circuit of claim 15, wherein the input stage includes an input transistor configured as a diode and connected between the input terminal and a power supply rail of the circuit, thereby establishing a gate-source voltage and a drain-source voltage of the input transistor corresponding to the input current, and wherein the current stage includes a bias current stage having a first transistor adapted to produce the bias current, the first transistor having a gate connected to the input terminal to establish a gate-source voltage of the first transistor equal to a gate-source voltage of the input transistor, and a second transistor connected to the first transistor in a cascode configuration and adapted to maintain a source-drain voltage of the first transistor equal to the source-drain voltage of the input transistor in response to the second bias voltage such that the bias current produced by the first transistor is proportional to the input current.

22. (new) The integrated circuit of claim 15, wherein the input stage includes an input transistor configured as a diode and connected between the input terminal and a power supply rail of the circuit, thereby establishing a gate-source voltage and a drain-source voltage of the input transistor corresponding to the input current, and wherein the current stage includes a main mirror current stage having a first transistor adapted to produce the main mirror current, the first transistor having a gate connected to the input terminal to establish a gate-source voltage of the first transistor equal to a gate-source voltage of the input transistor, and a second transistor connected to the first transistor in a cascode configuration and adapted to maintain a source-drain voltage of the first transistor equal to the source-drain voltage of the input transistor in response to the second bias voltage such that the main mirror current produced by the first transistor is proportional to the input current.

23. (new) The integrated circuit of claim 15, further comprising:

an input resistor connected between a first power supply rail at a first power supply voltage and the input terminal of the bias circuit, to set a value of the input current supplied to the input terminal, wherein the input stage is connected between the input terminal and a second power supply rail at a second power supply voltage, the input stage being adapted to provide a voltage drop between the input terminal and the second power supply rail approximating a voltage drop across a single diode, whereby the input stage minimizes sensitivity of the circuit to fluctuations in the first power supply voltage.

24. (new) The integrated circuit of claim 23, wherein the input stage is a transistor configured as a diode connected between the input terminal and the second power supply rail.

25. (new) The integrated circuit of claim 15, wherein the bias circuit further comprises:

a start-up stage adapted to provide a trickle-current to the reference bias stage to force the bias circuit into a stable operating condition.

26. (new) The integrated circuit of claim 25, wherein the start-up stage is adapted to reduce the trickle current from an initial current value to a final current value in response to a rise in the second bias voltage established by the reference bias stage.

27. (new) The integrated circuit of claim 25, wherein the start-up stage includes one of a resistor connected between a terminal common to both the feedback stage and the reference bias stage and a power supply rail, and a plurality of transistors having their respective source-drain current paths connected in series with one another, the series connected source-drain paths being connected between a power supply rail and a terminal common to both the feedback stage and the reference bias stage.

28. (new) The integrated circuit of claim 15, wherein the bias circuit further comprises:

a shut-down stage adapted to selectively enable and disable the supply of the input current to the input terminal so as to selectively enable and disable an operation of the bias circuit, respectively.

29. (new) The integrated circuit of claim 28, wherein the shut-down stage includes a transistor having a source-drain path connected to the input terminal and being adapted to shunt the input current away from the input terminal so as to disable the operation of the circuit in response to a control voltage applied to a control electrode of the transistor.

30. (new) A circuit for establishing a plurality of bias voltages suitable for biasing current sources from an input current, comprising:

means for supplying an input current;

means for establishing a first bias voltage in response to the input current;

means for producing a bias current proportional to the input current in response to the first bias voltage and a second bias voltage;

means for producing a main mirror current proportional to the input current in response to the first bias voltage and the second bias voltage;

means for producing a feedback current proportional to the input current in response to the bias current and the main mirror current; and

means for establishing the second bias voltage in response to the feedback current, whereby the first and second bias voltages track the input current over variations

in at least one of a temperature of the circuit and a power supply voltage provided to the circuit.

31. (new) The circuit of claim 30, wherein third and fourth bias voltages are established in response to the bias current and the main mirror current, and wherein the feedback current is produced in response to the third and fourth bias voltages.

32. (new) The circuit of claim 30, further comprising:

means for supplying a trickle current to establish a stable operating condition of the circuit.

33. (new) The circuit of claim 32, further comprising:

means for reducing the trickle current from an initial current value to a final current value in response to a rise in the second bias voltage indicative of the stable operating condition.

34. (new) A method of establishing a plurality of bias voltages suitable for biasing current sources from an input current supplied to a bias circuit, comprising:

(a) establishing a first bias voltage in response to an input current;

(b) producing a bias current proportional to the input current in response to the first bias voltage and a second bias voltage;

(c) producing a main mirror current proportional to the input current in response to the first bias voltage and the second bias voltage;

(d) producing a feedback current proportional to the input current in response to the bias current and the main mirror current; and

(e) establishing the second bias voltage in response to the feedback current of step (d), whereby the first and second bias voltages track the input current over variations in at least one of a temperature of the bias circuit and a power supply voltage provided to the bias circuit.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 15-34 are pending in the application, with 15, 30 and 34 being the independent claims. Claim 1 is sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Claims 2-14 were sought to be cancelled without prejudice to or disclaimer of the subject matter therein by a preliminary amendment filed on October 7, 2003. New claims 15-34 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Double Patenting Rejection

On page 2 of the Office Action, the Examiner rejected claims 1-14 under the judicially created doctrine of obviousness-type double patenting. Applicant has cancelled claims 1-14 without prejudice to or disclaimer of the subject matter therein. Thus, the rejection of claims 1-14 is moot.

New Claims 15-34

Applicant has added new claims 15-34. These claims contain patentable features over the inventions claimed in U.S. Patent No. 6,531,923 and U.S. Patent No. 6,714,080, to which the present application claims priority. Applicant is submitting herewith a terminal disclaimer in compliance with 35 CFR 1.321(c) to preclude an obviousness-type double patenting rejection and to be responsive to the double patenting rejection made by the Examiner in the Office Action mailed on March 1, 2004.

Support for new claims 15-34 is contained throughout the entire specification of the present applicant. For example, see in particular, figures 2-5 of the present application and the written description thereof, and claims 1-10, 15, 16, 18-20, and 22-23 of U.S. Patent No. 6,531,923, which is incorporated into the present application by reference.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will

expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Virgil L. Beaston
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Date: 9/1/04

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,982,602 B2
APPLICATION NO.: 10/679,269
ISSUE DATE : January 3, 2006
INVENTOR(S) : Lawrence M. BURNS

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim 16, at column 15, line 20, "the current in response" is replaced with

- - the input current in response - -.

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